Surpassing the Resistance Quantum with a Geometric Superinductor

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Superinductors have a characteristic impedance exceeding the resistance quantum \( R_Q \approx 6.45 \, \text{k}\Omega \), which leads to a suppression of ground-state charge fluctuations. Applications include the realization of hardware-protected qubits for fault-tolerant quantum computing, improved coupling to small-dipole-moment objects, and the definition of a new quantum-metrology standard for the ampere. In this work, we refute the widespread notion that superinductors can only be implemented based on kinetic inductance, i.e., using disordered superconductors or Josephson-junction arrays. We present the modeling, fabrication, and characterization of 104 planar aluminum-coil resonators with a characteristic impedance up to 30.9 k\( \Omega \) at 5.6 GHz and a capacitance down to \( \leq 1 \, \text{fF} \), with low loss and a power handling reaching \( 10^8 \) intracavity photons. Geometric superinductors are free of uncontrolled tunneling events and offer high reproducibility, linearity, and the ability to couple magnetically—properties that significantly broaden the scope of future quantum circuits.

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I. INTRODUCTION

In recent years, the field of superconducting quantum circuits has been introduced to a new player: the superinductor [1,2]. It is defined as a circuit element with zero dc resistance and a characteristic impedance \( Z_C > R_Q = h/(2e)^2 \approx 6.45 \, \text{k}\Omega \). For many quantum applications, it needs to be initialized in its ground state, which requires a low-loss self-resonance in the gigahertz range.

Superinductor resonators affect their local quantum environment. In the ground state, a resonator’s dimensionless charge and phase fluctuations are impedance dependent and their ratio is given by \( \delta n/\delta \phi = R_Q/Z_C \). For this reason, superinductors have been identified as necessary to measure the dual element of the Josephson junction, the phase-slip junction [3], since the observation of locked phase-slip oscillations (dual Shapiro steps) relies on a suppression of charge fluctuations and resistive heating [4–6]. Such a measurement raises the prospect of a new quantum-metrology standard for current [7–9]. In addition, new qubits such as the fluxonium [10–12] and hardware-protected qubits [13,14] such as the 0–\( \pi \) [1,15–18], as well as robust quantum error-correction schemes [19], are dependent on reliable low-loss superinductors.

High-characteristic-impedance resonators with fundamental frequency \( f_0 \) and low stray capacitance \( C \) give rise to large zero-point voltage fluctuations \( V_{ZPF} = \sqrt{\hbar f_0/(2C)} = 2\pi f_0\sqrt{\hbar Z_C}/2 \). The use of a superinductance can therefore boost conventional coupling limits in circuit QED [20,21] and facilitate coupling to hybrid piezoelectric components [22], as well as to systems having small electric dipole moments, such as electrons in quantum dots [23] and polar molecules [24]. Microwave optomechanics experiments such as ground-state cooling [25] and wavelength conversion [26] benefit from large \( V_{ZPF} \) but also require parametric coupling, which is increased by a strong coherent drive that relies on a high degree of linearity of the inductance [27].

To date, implementations of superinductors have been based on kinetic inductance, either by fabricating Josephson-junction arrays [10,28–31] or using highly disordered materials, such as nanowires [12,32–34] or granular aluminum [11,35,36]. Geometric inductances are widely considered to be unsuitable as superinductors, since reaching \( Z_C > R_Q \) has been argued to be impossible [2,10,28,36]. With a simple single-wire resonator, the characteristic impedance will indeed be bounded to approximately the impedance of free space \( Z_0 = \sqrt{\mu_0/\epsilon_0} = 377 \, \Omega \). In this paper, we exceed this limit by almost 2 orders of magnitude by making use of the mutual-inductance contribution of concentric loops in the form of a planar coil together with drastic miniaturization and substrate engineering.

II. PROOF OF CONCEPT AND MODEL

The geometric impedance of a straight wire according to the transmission-line model [37] is length independent and is defined by

\[
Z_{\text{wire}} = \frac{1}{\pi} \sqrt{\frac{\mu_0}{\epsilon_0 \epsilon_r}} \arccosh(d/w),
\]

where \( \arccosh \) is the inverse hyperbolic cosine function, and \( d \) and \( w \) are the diameter and width of the wire, respectively.
where \( w \) is the width of the wire and \( d \) is the distance to ground. One could try to increase \( Z_{\text{wire}} \) by increasing \( d \), but once \( d \) is in the order of the wavelength, the circuit starts to radiate energy, as if it is shunted by a load resistance \( Z_0 \) at resonance [2]. However, by winding the single wire in a planar and circular spiral form, the geometric inductance is enhanced, as expressed by the current-sheet method formula [38,39]

\[
L_g = \frac{\mu_0 n^2 d_{av}}{2} (\ln(2.5/\rho) + 0.2\rho^2),
\]

where \( \mu_0 \) is the vacuum permeability (assuming that none of the materials have magnetic properties), \( n \) is the number of turns, \( d_{av} = \frac{d_{in} + d_{out}}{2} \) is the average between the inner and the outer diameter of the coil, and \( \rho = (d_{out} - d_{in})/(d_{out} + d_{in}) \) is the fill ratio of the coil, which for our geometries is close to unity. As \( d_{out} \) is linear in the number of turns, Eq. (2) shows that the geometric inductance increases as \( L_g \sim n^3 \).

From the analytical model in Ref. [40], an expression for the fundamental resonance of a planar circular coil can be calculated as

\[
f_g = \frac{c_0}{\sqrt{\varepsilon_{\text{eff}} \pi (d_{in} + 2np)^2}},
\]

where \( \xi \) is a shape-dependent constant (for circular coils, \( \xi = 0.81 \)), the pitch \( p \) is the distance between adjacent turns (the wire width plus spacing), \( \varepsilon_{\text{eff}} \) is the effective relative permittivity, \( n \) is the number of turns, and \( c_0 \) is the speed of light in vacuum. Equation (3) is based on purely geometric considerations that are valid for \( n \gg 1 \) and \( \rho \approx 1 \) and it shows the resonance scaling as \( f_g \sim n^{-2}p^{-1} \sim l^{-1} \) [41], where \( l \) is the wire length, similar to a distributed-element resonator. Modeling the coil as a simple \( LC \) oscillator, we can express the impedance as \( Z_C = \sqrt{L/C} = 2\pi f_0 L \) and conclude that the characteristic impedance scales with the number of turns \( Z_C \sim n \) and that the parasitic capacitance of the inductor is linear in the coil radius \( C \sim np \).

The favorable scaling of the impedance and resonance of a coil with respect to a straight wire can be seen in Fig. 1(a). While the frequency of the wire \( (f_0 = c_0/2l) \) and the coil [Eq. (3)] scale similarly with respect to length, the impedance of the coil is increasing as \( Z_C = 2\pi f_0 L_g \sim \sqrt{l}/p \). The plot shows that the theoretical limit that constrains the characteristic impedance of the straight wire is lifted for the coil and that the superinductor regime is attainable with a fundamental frequency in the gigahertz range.

Figure 1(b) highlights the distributed-element behavior of the coil resonator. It displays the current distribution of a coil as a function of radius \( r \) taken from a finite-element-method (FEM) simulation and that of a \( \lambda/2 \) resonator \( I(r) = I_0 \sin(\pi(2r/d_{out})^2) \) [40], which neglects mutual inductance between turns.

Figure 1(c) compares the simulated frequency-dependent admittance of a coil shunted with a single lumped port and that of a simple \( LC \) circuit \( Y(f) = i2\pi fC + 1/(i2\pi fL) \). The first zero crossing represents the fundamental frequency of the coil. The capacitance can be extracted [42] by taking the derivative of the imaginary part of the admittance at that frequency, \( C = (1/4\pi)(d\varepsilon/df) \text{Im}(Y)|_{f=f_0} \), and we find that the resulting inductance \( L_g = 1/[C(2\pi f_0)^2] \approx 163 \text{ nH} \) is consistent with Eq. (2), for the same coil, i.e., \( L_g \approx 173 \text{ nH} \). We obtain a similar agreement, i.e., \( L_g \approx 180 \text{ nH} \), by extracting \( f_0 \) and its derivative \( df_0/dC \) from the simulated \( S_{11} \) parameter of a weakly coupled wave port,
in direct analogy to the experimental situation shown in Fig. 2(b).

The two admittance curves in Fig. 1(c) match in the dark shaded area, beyond which adding more LC series circuits to the model increases the accuracy up to the desired frequency (see the insets). This certifies that one can consider the coil as an ideal LC oscillator with a characteristic impedance of $Z_C$ up to and beyond its first resonance. Furthermore, below its fundamental frequency, the coil has a negative imaginary admittance, making it an ideal inductor. The assertions made in the rest of this paper will pertain only to the frequency region in which the LC approximation is valid.

III. DESIGN AND FABRICATION

It follows from Eqs. (2) and (3) and the relation $Z_C = \frac{2\pi f_0}{L}$ that the characteristic impedance of a coil can be made larger than $R_Q$ simply by adding turns; this, however, decreases $f_0$, which scales as $l^{-1}$. In order to keep the self-resonance in the gigahertz regime, we rely on two tactics. First, we reduce the pitch to maximize the turn-number-to-length ratio and therefore the characteristic impedance per unit length. Second, we reduce the $\varepsilon_{\text{eff}}$ of the substrate, which lowers the capacitance without affecting the inductance of the coil.

Regarding the second point, we fabricate coils formed by an evaporated 100-nm-thick aluminum wire, as shown in Figs. 2(a)–2(c), on three different substrates, i.e., (i) high-resistivity silicon (Si), (ii) 220-nm silicon membrane separated from a silicon handle wafer by 3 $\mu$m of vacuum (silicon on insulator, SOI), and (iii) a fully suspended 220-nm silicon membrane (SOI back-etched, SOI-BE) (for details, see Appendix A). For each substrate, we fabricate several coils with different $n$ and $p$ values and measure their $f_0$, internal ($Q_i$), and external ($Q_e$) quality factors in a dilution refrigerator, as shown in Fig. 2(d) and further discussed in Appendix B.

IV. LOSS, LINEARITY, AND KINETIC INDUCTANCE

We characterize a reference device on SOI-BE with a pitch of 300 nm, 155 turns, a first resonance at 4.55 GHz, and a geometric inductance of 933.9 nH. It is an average $Q_i$ device for the SOI-BE coils that are measured with additional radiation shielding, a comparably high $Q_e \approx 10^5$, and an optimized vapor-hydrofluoric-acid (VHF) release. Figure 3(a) shows the typical dependence of $Q_i$ as a function of the intraresonator photon number $n_p$. From the fit to a two-level-system (TLS) model (for details, see Appendix C), we extract an effective-loss tangent $F \cdot \delta_{\text{TLS}} = 1.3 \times 10^{-5}$. The best device with $p = 200$ nm shows about 10 times lower loss, on a par with state-of-the-art millimeter-sized coplanar waveguide resonators on sapphire [43]. Generally speaking, for stronger waveguide coupling, we...
observe lower values of $Q_i$. However, for $Q_e \geq 5 \times 10^4$, the high power $Q_i$ is consistently above 10$^6$. The full range of values can be found in Table I.

The inset in Fig. 3(a) shows the degree of nonlinearity of the resonance. From a linear fit, we extract a frequency shift of $\delta f = f_0(n_p) - f_0(0)$ = 0.24 mHz per photon. At even higher powers, typically $10^6 < n_p < 10^8$, the Lorentzian shape of the resonance starts to distort, indicating the onset of a breakdown of superconductivity.

In order to quantify the effect of kinetic inductance, we perform temperature sweeps on the same device. Figures 3(b) and 3(c) show its frequency shift $\delta f(T) = f_0(T) - f_0(0)$ and quality-factor degradation $\delta Q_i^{-1}(T) = Q_i^{-1}(T) - Q_i^{-1}(0)$ as a function of the temperature $T$. This behavior can be accurately modeled using Mattis-Bardeen equations (see Appendix C). We extract a value of $L_k = 58.0$ nH, i.e., only 5.9% of the total $L$. From this value and the equation [44]

$$L_k = \mu_0 \lambda^2 L(0) \frac{l}{w h},$$

we infer a London penetration depth $\lambda_L(0)$ of 147 nm, where $\mu_0$ is the vacuum permeability and $l$, $w$, and $h$ are the length, width, and thickness of the wire. This number is henceforth used to estimate the small correction due to kinetic inductance for all coils.

V. CHARACTERISTIC IMPEDANCE AND CAPACITANCE

Figure 4 summarizes the data extracted from 104 different coils on three substrates. The first row shows the measured frequency data as a function of the number of turns $n$ for each substrate. The fits (lines) are taken from Eq. (3) with a correction to include the kinetic inductance

$$f_0 = f_g \sqrt{\frac{L_g}{L_g + L_k}},$$

where the only fit parameter is the effective permittivity $\varepsilon_{eff}$ in $f_g$. The second row in Fig. 4 shows the characteristic impedance obtained with $Z_C = 2\pi f_g L_g + L_k$, where $L_g$ and $L_k$ are calculated using Eqs. (2) and (4) and the
frequency \( f_0 \) is given by the data (points) and the fits to the data (lines) shown in the first row. The fits are in excellent agreement with the data points and we find \( \epsilon_{\text{eff}} \) values of 6.89 \( \pm \) 0.09 for silicon, 2.04 \( \pm \) 0.93 for SOI, and 1.25 \( \pm \) 0.19 for SOI-BE. In the case of silicon, \( \epsilon_{\text{eff}} \) can be estimated with \( \epsilon_{\text{eff}} = (\epsilon_{\text{Si}} + 1)/2 = 6.5 \), very close to the fit results, and in the case of SOI-BE we find a value close to that of vacuum. The total inductance \( L \) is calculated to be in the range 35–992 nH, while the coil capacitance \( C \) is in the range 0.88–7.71 fF. A detailed summary can be found in Table 1.

Figure 5 compares the effects of reducing \( \epsilon_{\text{eff}} \) and the pitch on \( C \) and \( Z_C \). A reduction of \( \epsilon_{\text{eff}} \) has the effect of decreasing the capacitance, while the inductance remains unchanged, as all substrates have \( \mu_r = 1 \). We find that \( C \) scales linearly with the coil radius \( r \approx np \), in agreement with the expected scaling \( C \sim np \) derived earlier. In the limit of a large filling factor \( \rho \approx 1 \) and \( n \gg 1 \), the simplification \( r = np \) is valid and the self-capacitance of a coil can simply be estimated based on its outer radius for a given substrate, highlighting the importance of miniaturization.

In order to quantify the capacitance suppression, we extract the constant gradient \( dC/dr \) for each pitch \( p \) and each substrate, resulting in a total of nine data points. The extracted gradients are approximately pitch independent and are therefore averaged for each substrate, resulting in the three values reported in Fig. 5(a). The exception is the SOI substrate, which exhibits a strong pitch dependence (inset), leading to the large 90\% confidence interval of \( \epsilon_{\text{eff}} \) reported earlier. The reason is that coils with larger \( p \) have a larger size and an electric field distribution with a larger fraction residing in the silicon handle wafer. Moreover, the electric field rapidly decays in the vertical direction, resulting in a large improvement obtained by changing the substrate from silicon to SOI, as can be seen in Figs. 5(a) and 5(b). Simulations suggest that the capacitance suppression saturates for a vacuum gap of around 20 \( \mu \)m, depending on the overall coil size.

The data presented in Fig. 5(b) show the characteristic impedance for measured coils with a similar fundamental frequency \( f_0 = (10.7 \pm 0.3) \) GHz. The superlinear improvement obtained by going to lower pitches occurs because fixing the frequency has the effect of approximately fixing the wire length. For a set length, lower-pitch coils have more turns, which gives higher inductance and smaller radii for lower parasitic capacitance. Both have the effect of boosting the characteristic impedance. The dashed lines represent analytical expressions derived from Eqs. (2), (4), and (5) and the bands correspond to the error of \( \epsilon_{\text{eff}} \) as discussed earlier. In the case of SOI, the \( \epsilon_{\text{eff}} \) value is interpolated between different pitches, resulting in a slightly modified shape and a narrow error band.

VI. CONCLUSIONS

In this work, we show that suspended aluminum coils represent linear low-loss geometric superinductor resonators that can be used as an ideal superinductance below their self-resonance frequency. We are able to show...
that $Z_C \approx 5 \times R_Q$, about 80 times the previously claimed limitation for geometric inductors, $Z_0$.

Such a highly miniaturized microwave resonator with large zero-point voltage fluctuations reaching $V_{ZPF} \approx 50 \, \mu\text{V}$, which maintains a linearity of up to $10^8$ photons, is an attractive platform for hybrid devices. With losses as low as $Q_1 \approx 8 \times 10^5$ at single-photon powers despite the small gap sizes on the order of 100 nm, it will also find applications for new quantum circuits that require a high degree of parameter control and top-down fabrication reproducibility, such as fluxonium and 0–π qubits in new error-protected regimes. Such applications will require a connection to the center of the coil and initial numerical and experimental results confirm that this is possible with low loss and an additional stray capacitance as low as 0.1 fF using the air-bridge process introduced in Refs. [25,45].

Most importantly, and in contrast to circuit elements based on kinetic inductance, the geometric superinductance is a true single-wave-function superconducting device. This rules out the possibility of charge offsets that could impede the visibility of dual Shapiro steps [46], as well as uncontrolled phase- and charge-tunneling events that might become limiting factors for the dephasing times of multiterminal qubits [47,48]. In addition, one can obtain strong magnetic coupling to feed lines or other resonators without significantly increasing the parasitic capacitance, as required for certain error-protected readout and control schemes [15,17].

Our study provides simple analytical models to guide future design choices in such applications. Specifically, we find a simple way to predict the coil self-capacitance that only relies on knowledge of the radius and substrate. Potential challenges include increased flux noise due to the large perimeter of the coil [49], which can be addressed with new materials [50] or improved surface-fabrication techniques. For example, etching rather than lift-off might enable an even smaller coil pitch, with better interfaces and lower TLS losses resulting in even higher values of $Z_C$. Moreover, we believe that the presented design and fabrication methods could also help to reliably increase the $Z_C$ value of traditional superinductors.

The data and code used to produce the figures in this manuscript are available online [51].

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**APPENDIX A: DEVICE FABRICATION**

The devices are fabricated on three different substrates, as shown in Figs. 2(a)–2(c). In the case of silicon (Si), the fabrication consists of a single-layer process on a high-resistivity silicon wafer. The coil, ground, and waveguide are patterned by e-beam lithography (EBL) operated at 100 keV on a 300-nm-thick layer of CSAR 13 resist. An evaporation of 100 nm of aluminum at a rate of 1 nm/s in ultrahigh vacuum (UHV) is followed by a lift-off process in N-methyl-2-pyrrolidine (NMP) at 80 °C, resulting in the desired metallic pattern.

The fabrication on silicon-on-insulator (SOI) consists of a multilayer fabrication process. The wafer comprises a 220-nm-thick Si layer on 3 μm of silicon dioxide (SiO2), which rests on 750 μm of Si [45,52]. In the first step, EBL is used to pattern arrays of small holes (radius between 65 and 100 nm depending on the pitch) on the thin Si layer around the coil and on the waveguide. The chip is then mounted in an inductively coupled plasma (ICP) etcher, where C4F8 and SF6 etch the holes through the silicon layer, reaching the oxide, which acts as an etch stop. Then the coil is patterned and evaporated as in the previous case. The last step involves VHF etching (memsstar ORBIS ALPHA), in which the vapor penetrates through the etched holes and locally removes the oxide underneath, thus terminating the process with a suspended membrane.

The last fabrication routine, aimed at producing SOI back-etched (SOI-BE) samples, is developed, deploying a wafer similar to that used in the former procedure, but with the Si handle wafer lapped down to 200 μm. The first two steps are identical to the SOI process, with the difference that in this case no holes are patterned directly around the coils, as they are not needed to suspend the membrane. After the coil-metal deposition and consequent lift-off, a layer of 5 μm of LOR 5B resist is placed on the structures as protection for the following subprocesses. LOR 5B is chosen specifically because it does not dissolve in acetone, used in the next lift-off. A mask is written in EBL on the back side of the chip into 270 nm of PMMA 950k EL4, leaving open rectangles positioned directly under the coil. The rectangles are designed to be large enough for alignment not to be critical. A layer of 50 nm of chromium (Cr) is deposited and the consequent lift-off carried out by acetone at 40 °C. The chip is then mounted in an ICP with the devices facing down and the silicon in the rectangles is completely etched away with a customized Bosch process comprised of a gas mixture of C4F8 and SF6. This leaves only the SiO2 and 220-nm silicon layer under the coils. For the Cr to stick effectively throughout the etch process, the
bottom of the chip must have a low level of roughness. The resist is then removed via hot NMP and the oxide layer is locally etched by VHF. Finally, the coils are left suspended on a 220-nm membrane with vacuum below.

APPENDIX B: MEASUREMENT AND PARAMETER SUMMARY

The coils are coupled to a shorted waveguide, which guarantees inductive coupling, as shown in Fig. 2(b), where we are able to control the coupling strength by adjusting the distance with a resulting extrinsic quality factor $Q_i$ between $5 \times 10^3$ for a distance of a few micrometers and over $10^5$ for distances around a couple of times the coil size. Our model does not include parasitic capacitance or mutual inductance due to the coupling wire or the surrounding ground, which in principle can cause small negative and positive shifts in the coil frequency, respectively [53]. Nevertheless, the simulations indicate that these coupling-related shifts are below 1%.

We measure the complex $S_{11}$ parameter using the setup shown in Fig. 2(d) and fit the $I$ and $Q$ quadratures to a reflective model [25] to extract the external and internal quality factors, $Q_e$ and $Q_i$, and the first resonance frequency, $f_0$, for all coils as a function of the input power. We are confident that the measured values correspond to the fundamental mode resonance, since the wave-port-coupled FEM simulations of $f_0$ agree with the data to within 20%. Table I in the main text summarizes the important parameters of all measured devices.

APPENDIX C: TLS AND BCS FIT MODELS

Figure 3(a) in the main text shows the typical dependence of $Q_i$ as a function of the intraresonator photon number $n_P$, consistent with the presence of TLSs [54]:

$$Q^{-1}_{TLS} = F \delta_{TLS} \text{tanh}(h\omega/2k_BT) \left(1 + n_P/n_C\right)^\beta + Q^{-1}_{sat},$$

(C1)

where $F$ is the fraction of the electric field in the lossy material, $\delta_{TLS}$ is the TLS loss tangent, $n_C$ is the critical photon number that saturates the TLS, and $Q_{sat} = 1.1 \times 10^6$ represents any additional loss mechanisms. We extract $F\delta_{TLS}$ to be $1.3 \times 10^{-3}$. The exponent $\beta$ is commonly taken as 0.5 and the deviations indicate an interaction between TLSs [55]. For our system, $\beta$ is found to be 0.4, which implies some degree of interaction.

In order to quantify the effect of kinetic inductance, we perform temperature sweeps of the same device. Figures 3(b) and 3(c) in the main text show its frequency shift $\delta f (T) = f_0(T) - f_0(0)$ and quality-factor degradation $\delta Q^{-1}(T) = Q^{-1}_{0} - Q^{-1}_{0}(0)$ as a function of the temperature $T$. This behavior can be accurately modeled using BCS theory [56]:

$$\frac{\delta f (T)}{f_0(0)} = -\frac{\alpha \gamma}{2} \frac{\delta \sigma(T, \Delta)}{\sigma(T, \Delta)},$$

(C2)

and

$$\delta Q^{-1}(T) = \frac{\alpha \gamma}{2} \frac{\delta \sigma_i(T, \Delta)}{\sigma_i(T, \Delta)},$$

(C3)

where $\alpha = L_k/(L_0 + L_k)$ is the fraction of the kinetic inductance to the total inductance, $\gamma$ is a material-dependent parameter, which is $-1$ for aluminum thin films [54], and $\sigma_1$ and $\sigma_2$ are the real and imaginary parts of the conductance $\sigma = \sigma_1 - i\sigma_2$ as described in Ref. [56]. The data are fitted with $\alpha$ as a free parameter, while the gap voltage $\Delta$ is taken to be the bulk value for aluminum, which is shown to be valid for the used film thickness of 100 nm [57]. From the fit, we extract $\alpha = 5.9\%$, which results in a kinetic inductance of $L_k = 58.0$ nH. From this value and $L_k = \mu_0 \lambda_L^2(0)/(lwh)$, we infer the London penetration depth $\lambda_L(0) = 147$ nm [44], where $\mu_0$ is the vacuum permeability and $l$, $w$, and $h$ are the length, width, and thickness of the wire. The fact that the measured $\lambda_L(0)$ is significantly higher than the value for bulk aluminum (15 nm [54]) is likely due to the thin-film nature of the metal [58].


[39] Equation (2) yields accurate results with an error $\leq 8\%$ for thin-film planar circular air-core spiral inductors with $(p - w)/l \leq 3$ in the lumped-element limit [38].


[41] An approximated expression of the length of a circular spiral based on a series of concentric circles: $l \simeq \sum_{n=1}^{N} 2\pi r_n \simeq \sum_{n=1}^{N} 2\pi n / (n + 1/2) \simeq n^{2/3}$.


